IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Kevin M. Conley et al.		
Title:	Management Of Non-Volatile Memory Systems Having Large Erase Blocks		
Application No.:	10/749,831	Filing Date:	December 30, 2003
Examiner:	Eland, Shawn	Group Art Unit:	2188
Docket No.:	0084567-247US0	Conf. No.:	9380

Mail Stop Appeal Brief-Patents
Commissioner for Patents
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RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

In response to the Notification of Non-Compliant Appeal Brief dated July 17, 2009, the section on SUMMARY OF CLAIMED SUBJECT MATTER of the Appeal Brief is being re-submitted to the Board of Patent Appeals and Interferences. A petition for an extension of time is being submitted herewith to extend the time for response to October 19, 2009 (October 17 and 18 falling on a weekend.)

V. SUMMARY OF CLAIMED SUBJECT MATTER

INDEPENDENT CLAIM 2:

The claim is directed to a method of operation of a non-volatile memory system having blocks of memory cells that are simultaneously erasable. (For erasable blocks see application ¶0008 & ¶0045 & FIG. 3.) As background, Figure 3 of the present application shows individual planes (sub-arrays) 0 and 1 in a memory system. Each of the planes has its memory cells divided into sixteen such blocks 0-15. The blocks are in turn individually divided into a given number of pages of memory cells, sixteen pages 0-15 being shown in the block illustrated in Figure 4. Data are written (programmed) into a block in units of the page (a programmable unit; see application ¶0008 & ¶0046). As shown in the address tables of Figures 7A and 7B, the blocks of memory cells are identified by physical block numbers (PBNs), and blocks of data programmed into the designated physical blocks are identified by logical block numbers (LBNs). Pages of memory cells within physical blocks are identified by their offset positions within their blocks. (See, for example, page 0, page 1, etc. of the block of Figure 4.) Each page contains one or more units (such as sectors) of data received from a host (see application ¶0008 & ¶0046, and the example data sector shown in Figure 5).

When a large number of units of data with sequential logical addresses (i.e., logical sector numbers or page numbers) relative to the storage capacity of a memory cell block are received by the memory system for programming, it is efficient to program that data in an erased block of memory cells in sequentially addressed pages. This is because a block storing pages in sequential logical addresses is self-indexed.

However, when only one or a few host units of data have sequential logical addresses relative to the capacity of a memory cell block, it can be inefficient to program that small amount of data in an erased block, particularly when the received data have the same logical addresses as data already programmed and are therefore updating the original data. This is because it will make an otherwise sequential block no longer so. Therefore, data are programmed differently depending on the number of units of data having sequential logical addresses relative to the data storage capacity of a block of memory cells. For example, by handling the updating of a few pages differently (writing them to a first type of designated logical blocks, E1 instead of other type of logical blocks, such as E2, see FIG. 8 and FIG. 9), memory performance is improved

when small updates are being made. (See the Abstract and the Summary of the Invention section of the present application, ¶¶0015-0016.)

An example of programming a relatively small amount of data is illustrated in application Figure 9. (Described in application ¶¶0056-0058.) The independent claim 2 on appeal calls for "designating" or "allocating" one of the memory cell blocks for programming relatively small amounts of data having sequential logical addresses. Such a block is identified in the example of Figure 9 as the E1 block. Figure 9 shows an updated version of data stored in pages 7-10 of original block 3 being programmed into the next erased pages in order of the E1 block. It was chosen to program this amount of data into the designated E1 block, instead of some other block, because the number of pages of data falls below a pre-set proportion of the total number of pages within a block. Examples of this pre-set proportion include 50% and 75% (see application ¶¶0064-0066). In the example of Figure 9, the memory cell blocks have 16 pages of memory cells that can therefore store up to 16 pages of data, and 4 pages of updated data are being programmed. These 4 pages of data are programmed into the designated E1 block because their number is less than a pre-set proportion of 8 pages, using the 50% number given as an example in application ¶0065.

The pre-set proportion is specified by dependent claims 26, 27, 30, 33, 35, 37, 39 and 41 to be within a range of 25-75 percent of the storage capacity of a memory cell block. This is described in ¶0065 of the present application. Some of the appealed claims additionally call for programming larger numbers of units of data with sequential logical addresses into another designated block, called the E2 block in the present application. (See application ¶0015 & ¶0056, for example.)

INDEPENDENT CLAIM 28:

Independent claim 28 is similar to independent claim 2 in that it calls for "designating" or "allocating" one of the memory cell blocks E1 for programming relatively small amounts of data having sequential logical addresses (i.e., "when the a number of the units of data with sequential logical addresses is less than the pre-set fraction".) As in claim 2, such a block is identified in the example of Figure 9 as an E1 block. Thus, when the write data is such that satisfies the criterion for dE1 or E1 (Step 113, FIG. 19), it is written to the dE1 or E1 block (Steps 119 or 127, FIG. 19). Otherwise, it is written to another block (e.g., Steps 107, FIG. 19).

INDEPENDENT CLAIM 31:

Independent claim 31 is similar to independent claim 2 in that it calls for "designating" or "allocating" one of the memory cell blocks E1 for programming relatively small amounts of data having sequential logical addresses (i.e., when the a number of the units of data with sequential logical addresses is less than the pre-set fraction of said given number".) As in claim 2, such a block is identified in the example of Figure 9 as a dE1 or E1 block. Thus, when the write data is such that satisfies the criterion for dE1 or E1 (Step 113, FIG. 19), it is written to the dE1 or E1 block (Steps 119 or 127, FIG. 19). Otherwise, it is written to an E2 block (Step 107, FIG. 19, FIG. 8) if there is capacity (Steps 103, FIG. 19).

INDEPENDENT CLAIM 36:

Independent claim 36 is similar to independent claim 2 in that it calls for "designating" or "allocating" one of the memory cell blocks dE1 or E1 for programming relatively small amounts of data having sequential logical addresses (i.e., when the a number of the units of data with sequential logical addresses is less than a pre-determined fraction of said given number".) As in claim 2, such a block is identified in the example of Figure 9 as a dE1 or E1 block. Thus, when the write data is such that satisfies the criterion for dE1 or E1 (Step 113, FIG. 19), it is written to the dE1 or E1 block (Steps 119 or 127, FIG. 19), if there is capacity (Steps 117 or 125, FIG 19). Otherwise, it is written to another block (e.g., Steps 107, FIG. 19).

INDEPENDENT CLAIM 40:

Independent claim 40 is similar to independent claim 2 in that it calls for "designating" or "allocating" one of the memory cell blocks dE1 or E1 for programming relatively small amounts of data having sequential logical addresses (i.e., when the a number of the units of data with sequential logical addresses is less than a pre-determined fraction of said given number".) As in claim 2, such a block is identified in the example of Figure 9 as a dE1 or E1 block. Thus, when the write data is such that satisfies the criterion for dE1 or E1 (Step 113, FIG. 19), it is written to the dE1 or E1 block (Step 119, FIG. 19). Otherwise, it is written to an E2 block (FIG. 8) if there is capacity. If the E2 block does not have enough capacity, write it to an erase block (Steps 115, 107, FIG. 19).

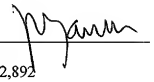
REMARKS

The Examiner has objected to the previous submission of the Appeal Brief where "the claimed invention does not separately refer to the independent claims 2, 28, 31, 36 and 40, which shall refer to the specification by page and line number and to the drawings, if any."

This has been corrected in the above replacement section labeled: V. SUMMARY OF CLAIMED SUBJECT MATTER.

FILED VIA EFS

Respectfully submitted,



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Date

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